ABSTRACT OF THE DISCLOSURE

A method of noise analysis and correction of noise violations for an integrated circuit design includes steps of (a) receiving as input a standard parasitic exchange file for an integrated circuit design; (b) parsing the standard parasitic exchange file to generate a resistance graph; (c) generating a representation of the resistance graph to determine noise critical nets; (d) generating a list of only noise critical nets from the representation of the resistance graph; (e) selecting a net from the list of only noise critical nets; (f) calculating a value of total crosstalk noise in the selected net from all aggressor nets relative to the selected net; and (g) generating as output the value of total crosstalk noise in the selected net for correcting a noise violation.